PATENT
Customer No. 22,852
Attorney Docket No. 6720.0103-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
MING-DOU KER et al.	Group Art Unit: Unassigned
Application No.: 10/626,601	Examiner: Unassigned
Filed: July 25, 2003	
For: MIXED-VOLTAGE CMOS I/O BUFFER WITH THIN OXIDE DEVICE AND DYNAMIC N-WELL BIAS CIRCUIT	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. To the undersigned's knowledge, this Information Disclosure Statement is being filed before the mailing date of a first office action on the merits for the above-identified application.

Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the listed documents and indicate that they are considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

documents as prior art against any claim in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: October 29, 2003

By: Robert J. Rotatt Reg 24,014
Yitai Hu
for Reg. No. 40,653

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.:	0678-0103	Appln. No.:	10/626,601
Applicants:	MING-DOU KER et al.		
Filing Date:	July 25, 2003	Group:	Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Dat If Appropriate
		5,864,243	01/26/1999	Chen et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Marcel J. M. Pelgrom and E. Carel Dijkmans, "A 3/5 V Compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol. 30, no. 7, July 1995, pp. 823-825
	M. Takahashi, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsuda, "3.3V-5V Compatible I/O Circuit Without Thick Gate Oxide," Proc. of IEEE Custom Integrated Circuits Conference, 1992, pp. 23.3.1-23.3.4
	G. Singh and R. Salem, "High-Voltage Tolerant I/O Buffers With Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol. 34, no. 11, 1999, pp. 1512-1525
	Deng-Yuan Chen, "Design of a Mixed 3.3V and 5V PCI I/O Buffer," Proc. of ASIC, 1996, pp. 336-339

Examiner	Date Considered
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce